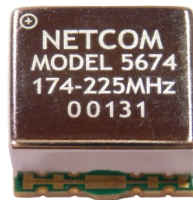


Specifications



FEATURES

Netcom's 5674 tunable filter covers the frequency range of 174MHz to 225MHz.

The filter is a single band tunable filter offering the advantage of small size with a control system comparable to larger size filters.

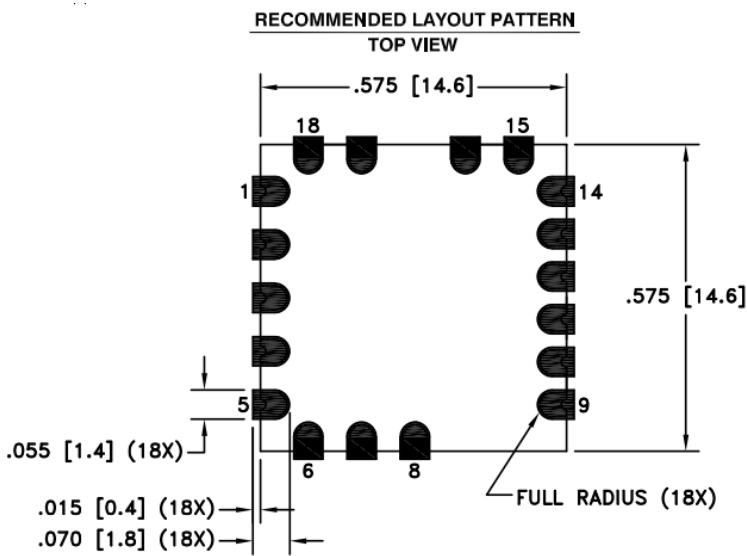
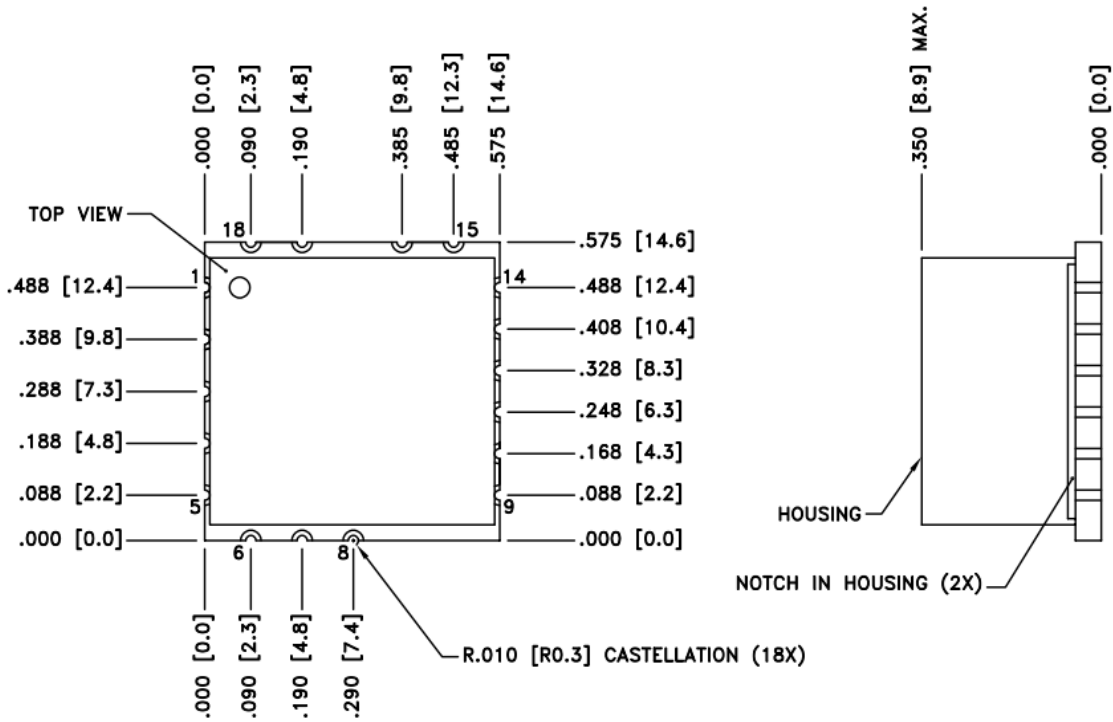
The following table shows the typical performance of the filter.

Frequency Range	174MHz to 225MHz
BW (Typical)	6.5%
Impedance (Input /Output) - Typical	50 Ω
Ftune +/- 10% Rejection	< -17dB
Ftune +/- 15% Rejection	< -24dB
Ftune +/- 20% Rejection	< -29dB
Tuning Speed	< 35 μ s
Insertion Loss (Typical)	4.7dB
Tuning Resolution*	500KHz
P1dB	+24dBm
Max Power Handling	+28dBm
IIP3	+39dBm
DC Power - Typical Max	3.3 Volts 30 mA
Operating Temperature Range	-40 to +85°C
Control Interface	Serial Input
Dimensions	0.575 x 0.575 x 0.350 inches

*See page 3 for details

Note: Parameters subject to change

Mechanical



- NOTES:
1. TOLERANCES ± 0.010 [0.25] UNLESS OTHERWISE SPECIFIED.
 2. DIMENSIONS ARE INCHES [mm].

PIN DESIGNATORS	
PIN NUMBER	DESCRIPTION
1	RF_IN
2	GND
3	SPI_CLK
4	SPI_MOSI
5	NC
6	NC
7	NC
8	NC
9	NC
10	NC
11	NC
12	TUNE_READY
13	GND
14	RF_OUT
15	GND
16	VCC (+3.3V)
17	SPI_CS
18	GND

NC = NO CONNECT

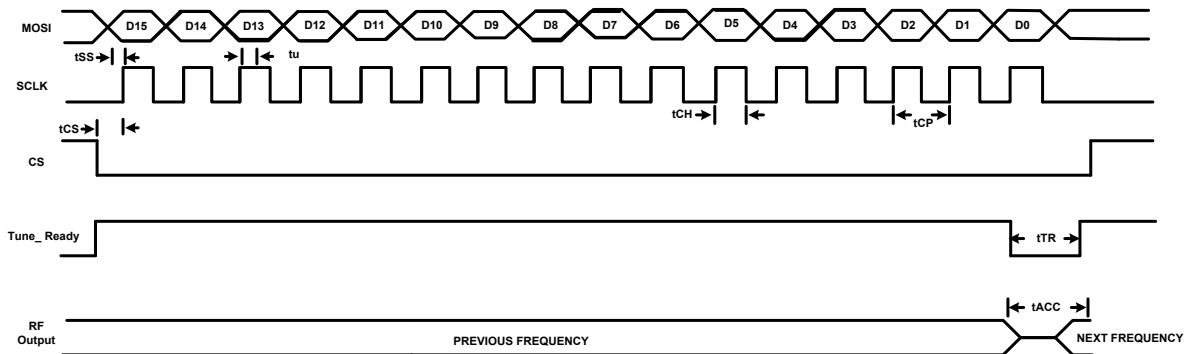
Serial Address Input Timing Diagram

Tuning resolution is 500KHz from address 1392 decimal (174.000MHz) to 1800 decimal (225.000MHz) .
 Tuning of the filter starts when the last data clock (16th) pulse of the address is sent to the unit while the CS (Chip select) is low.

The filter will move to the correct tune channel which allows the tuned address frequency to pass while meeting all of the tuning parameters. In some cases the filter tune channel may not move.

Symbol	Parameter	Min	Max	Units
tSS	Setup time MOSI Data to SCLK*	50		ns
tu	Hold Time MOSI Data From SCLK		0	ns
tCH	Clock High Time	125		ns
tCP	Clock Period	250		ns
tCS	Chip Setup Time (CS falling edge to SCLK start)	125		ns
tTR	Tune_Ready indicator***		35	us
tACC	Access time from Last (16th) SCLK edge to Fo**		35	us

56XX ADDRESS PROTOCOL



* Data clocked in on SCLK leading edge.

** Filter tunes to address on last clock bit of address SCLK.

*** Tune_Ready at logic low when filter processing tuned address.

Environmental Specification Standards

Temperature:

- High temperature shall meet MIL-STD-810E, Method 501.3, Procedure I to 125°C storage, and procedure II to 85°C operating.
- Low temperature shall meet Method 502.3, Procedure I to -57°C storage, and Procedure II to -40°C operating.

Vibration:

- MIL-STD-810E Method 514.4

Shock:

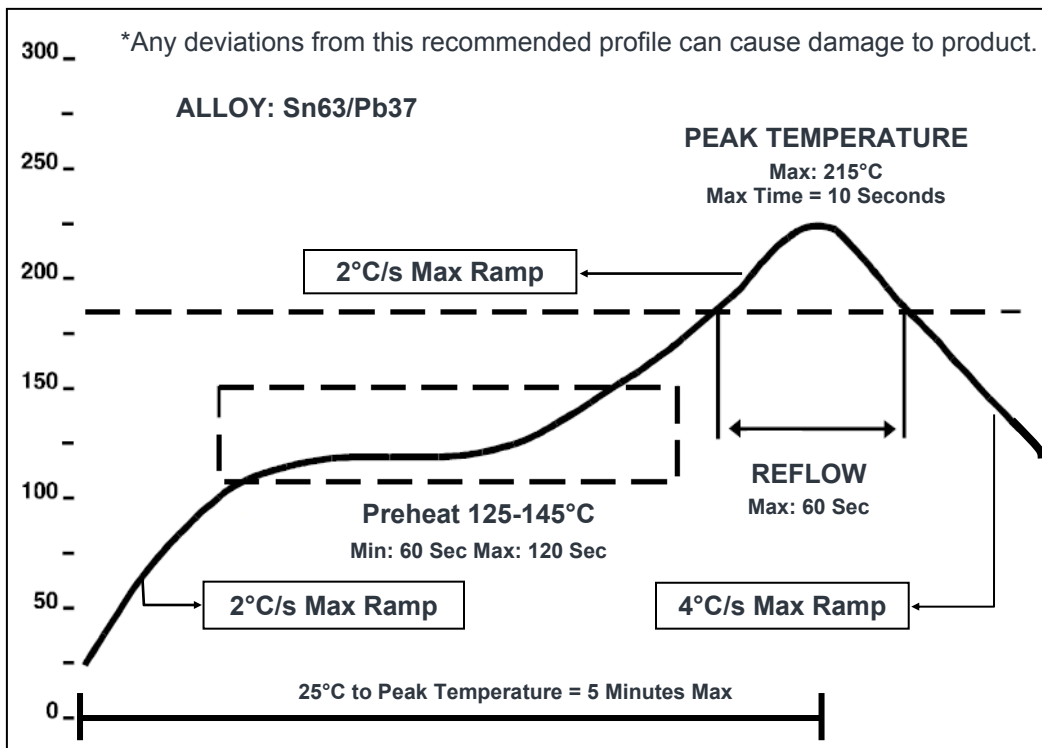
- MIL-STD-810E Procedure VI, Method 516.4

Solder Process

Filter model 5674 is designed for system assembly through SMT reflow soldering. All filter components have been selected for secondary reflow and are assembled using SAC305 high temp solder. The system level SMT reflow temperature profile is as specified in the IPC/JEDEC J-STD-020 standard for a Sn-Pb Eutectic Process. In systems using Pb-Free and high temp solder, the filter must be mounted through a hand soldering process.

The exact reflow profile required will depend on the characteristics of the circuit board assembly like thickness, size, and heat transfer. Also affecting the reflow profile is the solder paste type, flux, and density of other components. Temperature limitations of other components on the circuit board also must be considered. The recommended profile below is at the printed circuit board interface using Sn63/Pb37 tin lead solder.

Recommended Solder Profile



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